

Field Effect Transistor (FET) Device and Method of Fabricating Thereof

Seeking parties interested in licensing and commercialization of technology.

Technical Applications

This technology is primarily applied in advanced high-density semiconductor integrated circuits, sub-nanometer logic node fabrication, and low-power microelectronics. Key application areas include high-performance computing processors, mobile system-on-chip (SoC) devices, memory arrays, wearable technology, and IoT edge controllers where compact form factor, low off-state leakage, and superior electrostatic channel control are critical.

Salient Features

- ✓ C-Shaped Nanosheet Channel Architecture
- ✓ Enrobed Hafnium Oxide Dielectric Layer
- ✓ Streamlined Fabrication Method

Technology Brief

This technology relates to a novel Field Effect Transistor (FET) device and its fabrication method, designed to optimize electron flow and channel control. The structure features a silicon substrate supporting a vertically positioned gate terminal along with one or more C-shaped silicon nanosheets attached to the gate. Each C-shaped nanosheet is enrobed in a high-k hafnium oxide (HfO₂) layer to provide robust dielectric insulation. Integrated with source and drain regions situated on adjacent sides of the nanosheets to inject and collect electrons, this dual-channel C-shaped nanosheet architecture significantly enhances gate control, reduces leakage current, and ensures efficient carrier transport across the individual conduction channels.

Glimpse of the Technology



REFERENCE NUMBER

iTNT-TECH-0188



TECHNOLOGY SECTOR

Electronics & Semiconductors



IP STATUS

Patent Granted



APPLICATION NUMBER

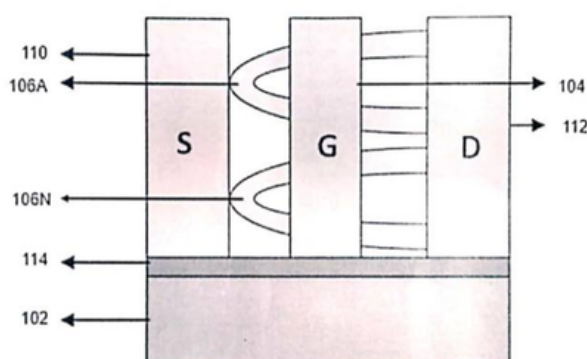
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TECHNOLOGY READINESS LEVEL

TRL 3

Block Diagram



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